A Fully Integrated Broad-Band Amplifier MMIC Employing a Novel Chip-Size Package

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***Abstract*—In this work, we used a novel RF chip-size package (CSP) to develop a broad-band amplifier monolithic microwave integrated circuit (MMIC), including all the matching and biasing components, for Ku- and K-band applications. By utilizing an anisotropic conductive film for the RF-CSP, the fabrication process for the packaged amplifier MMIC could be simplified and made cost effective. STO ($SrTiO_3$) capacitors were employed to integrate the dc biasing components on the MMIC. A novel pre-matching technique was used for the gate input and drain output of the FETs to achieve a broad-band design for the amplifier MMIC without any loss of gain. To improve the circuit stability of the amplifier MMIC in the out-of-band, a parallel RC circuit was employed at the input of the amplifier MMIC. The packaged amplifier MMIC exhibited good RF performance and stability over a wide frequency range. This work is the first report of a fully integrated CSP amplifier MMIC successfully operating in the Ku-/K-band.**

***Index Terms*—Anisotropic conductive film (ACF), broad-band amplifier, chip-size package (CSP), monolithic microwave integrated circuit, STO.**

I. Introduction

PROMISING applications for GaAs technology include monolithic microwave integrated circuit (MMIC) chip sets for Ku/K multimedia satellite communications and fixed wireless access systems. Various Ku-/K-band MMIC amplifiers have already been reported in the literature [1]–[8]. However, for low-cost and high-performance Ku-/K-band MMIC amplifiers, the following considerations should be noted.

1) Recently, demands for fully integrated RF devices with a broad-band operating range have increased in the market for Ku-/K-band multimedia satellite communication [1], [2] and fixed wireless access systems. A number of articles concerning amplifier ICs for Ku-/K-band applications have already been reported, but most of them are for hybrid ICs that at least require biasing components on the boards. This has resulted in a high manufacturing cost, due to the large module size and the high assembly cost.
2) Until now, mainly bare chip MMICs have been reported, and most of the packaged MMICs developed for Ku-/K-band applications involved face-up MMICs that were mounted on surface mount ceramic packages [7]–[9]. However, this technology resulted in a large chip size, and the RF performance of the packaged MMICs was degraded slightly in the millimeter wave range due to the parasitic elements inherently existing in these packages.
3) For Ku-/K-band MMICs, circuit stability should be guaranteed over a wide frequency range (from dc to the operating band) to prevent any unwanted oscillation in the out-of-band region as well as in the operation band. Therefore, if possible, unconditional stability in the out-of-band region as well as in the operating band should be ensured for stable operation. This is especially important for fully integrated RF devices, because their input and output impedance are not adjusted by external biasing and matching components on the board.

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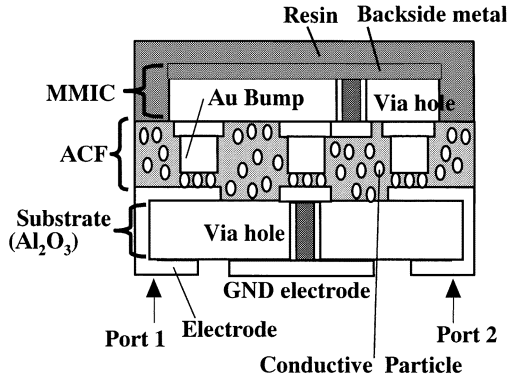

Fig. 1. Structure of the developed RF-CSP.

In this work, a fully integrated broad-band amplifier MMIC employing a novel RF chip-size package (CSP) was developed using a novel broad-band design technology.

We explain the characteristics of the novel CSP, give a detailed description of the CSP-based circuit design technology used for the amplifier MMIC, and elucidate a novel broad-band design technology that allows for good RF performance and circuit stability over a wide frequency range (Ku- and K-band).

II. RF-CSP

Fig. 1 shows the structure of the RF-CSP that we developed. A flip-chip GaAs MMIC is mounted on a 200-μm-thick Al_2O_3 substrate. The Al_2O_3 substrate was used because its coefficient of thermal expansion is an excellent match for that of GaAs. The electrode of the MMIC was electrically connected to the substrate electrode via an Au bump and conductive particles. The substrate electrodes (ports 1 and 2 in Fig. 1) were connected to the external signal lines. An external electrical ground was applied to the GND electrode of the substrate and was therefore

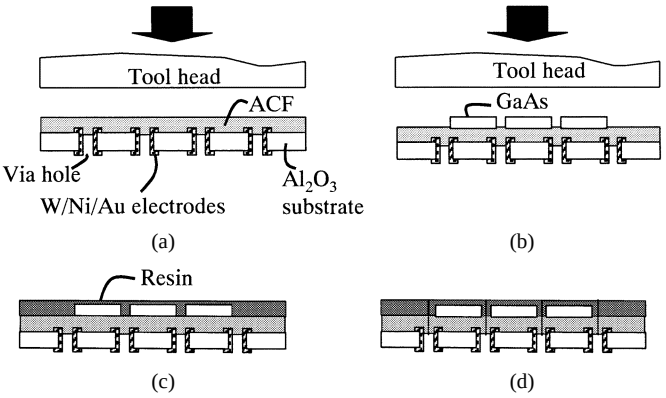

Fig. 2. Processing steps for the CSP MMIC.

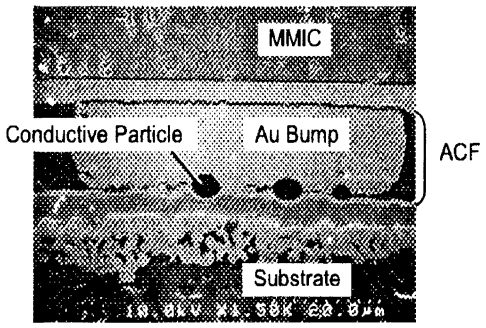

Fig. 3. Microphotograph of the interconnection between the MMIC and the substrate.

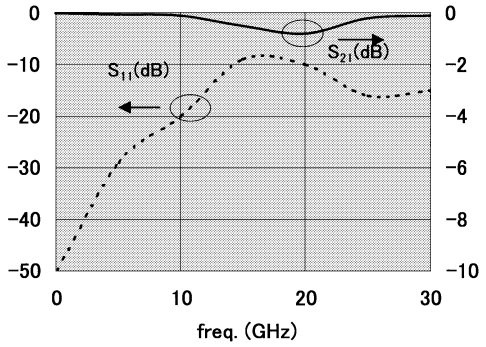

Fig. 4. Measured return and insertion loss of the RF-CSP at ports 1 and 2 of Fig. 1.

also supplied to the backside metal of the MMIC through the via hole in the substrate, the bump, and the via hole in the MMIC, as shown in Fig. 1. Therefore, the electrical ground for the passive and active components integrated on the MMIC is supplied by the backside metal through the via hole in the MMIC. The height and width of the Au bump are 15 and 45 μm, respectively. The backside of the GaAs MMIC was covered with a resin film. We adopted an anisotropic conductive film (ACF) for the under-filling material between the MMIC and the substrate, which makes the process of fabricating the RF-CSP very simple and cost effective. The ACF plays some important roles in the RF-CSP process, both for bonding and as an under-filled insulator. The ACF contains conductive particles that are 5 μm in diameter, and which are dispersed in a 30 μm thick insulating adhesive film. By using heat and pressure, the conductive particles form an electrical and mechanical bond between the bump on the MMIC and the electrode on the substrate, as shown in Fig. 1. In addition, the ACF also serves as an under-filled insulator between the MMIC and the substrate. Due to the ACF performing the above functions, processing the RF-CSP becomes very simple and cost-effective, because it removes the need for the bonding and under-filling processes that are required for conventional CSPs. Gold is the most suitable material for the conductive particles, but its high cost prevents its application to the process. Therefore, we used resin particles of 5-μm diameter that were coated with Ni–Au.

The steps used for processing the CSP MMIC are shown in Fig. 2(a)–(d). As shown in this figure, the process can be summarized as follows: prebonding, final bonding, encapsulation, and dicing. The ACF is first attached to the Al_2O_3 ceramic substrate with W–Ni–Au electrodes by heating with a tool head to about 100°C [Fig. 2(a)]. The multiple GaAs chips are then arrayed on the ACF, and are pressed together using a tool head at about 200°C [Fig. 2(b)]. During this process, the bonding between the bump on the GaAs MMICs and the electrodes on the ceramic substrate is also completed due to the conductive particles, without any additional bonding process taking place. The encapsulation process is required to protect the fragile GaAs MMICs from mechanical shock, and so the GaAs chips arrayed on the ceramic substrate are then covered with resin [Fig. 2(c)]. The ACF prevents the resin from flowing into the bottom of the ceramic substrate through the via holes during the encapsulation process. Finally, the ceramic substrate is divided into individual CSP MMICs by a dicing machine [Fig. 2(d)]. Fig. 3 shows the interconnection between the MMIC and the substrate after the above process was completed. In this work, the gold bumps were formed on the GaAs MMICs by an electroplating technology after the fabrication of the MMICs. Compared with conventional stud bump bonding (SBB) [10], the formation of multiple bumps and the adjustment of the height of the bumps is made possible by this method.

The RF-CSP was employed in the development of a broad-band amplifier. The input impedance of the RF-CSP was optimized to 50 Ω in the broad band. Fig. 4 shows the measured return loss (S_{11}) and insertion loss (S_{21}) of the RF-CSP at ports 1 and 2 of Fig. 1. To measure the return and insertion loss, a GaAs flip-chip MMIC with a 50-Ω micro-strip through-line was assembled in the package, as shown in Fig. 1. As shown in Fig. 4, the return loss (S_{11}) is less than -9 dB from 0 to 30 GHz. The maximum insertion loss between ports 1 and 2 (S_{21}) is -0.8 dB. The size of the RF-CSP is 2×3 mm^2.

III. Modeling of CSP-Based Passive Components for Circuit Design

If open-space modeling equations and equivalent circuits for all components are used for the CSP MMIC design, the RF performance of the MMIC deviates considerably from the design goals due to the underfill effect of the ACF. Therefore, in this work, the dielectric constant and the loss for the ACF including the conductive particles were determined by measurement. The measured dielectric constant and loss values were used for the EM simulation, and CSP-based modeling equations and CSP-based equivalent circuits were obtained for all of the

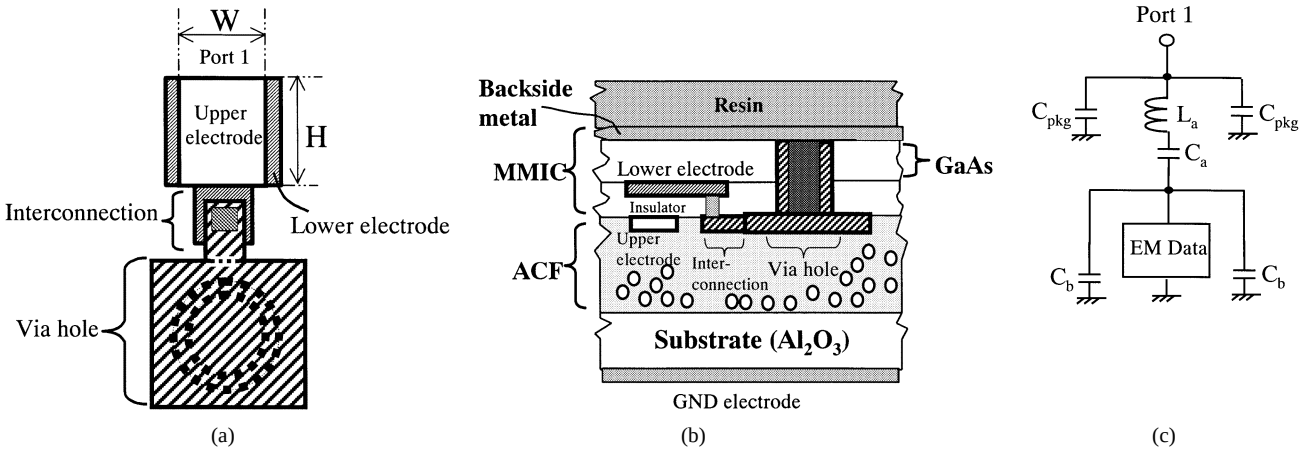

Fig. 5. (a) Plane view of the CSP-based MIM shunt capacitor. (b) Cross-sectional view of the CSP-based MIM shunt capacitor. (c) Lumped equivalent circuit of the CSP-based MIM shunt capacitor.

components from the EM simulation, reflecting the dielectric constant and loss measured for the ACF.

For the CSP-based striplines, the open boundary closed-form equation for microstrip [11] was employed to calculate the characteristic impedance of the striplines. As shown in Fig. 1, the structure of the CSP MMIC includes top and bottom ground planes (backside metal and the GND electrode), and therefore a new modeling equation for an asymmetric stripline structure containing two ground planes should be derived in order to obtain an accurate solution for the characteristic impedance. However, if the bottom ground plane (GND electrode) is located remotely from the MMIC, the stripline on the MMIC is equivalent to a microstrip with a single ground plane because the effect of the bottom ground plane can be ignored. According to EM simulation results, if the distance between the bottom ground plane and the MMIC is larger than 200 μm, the effect of the bottom ground plane can be ignored, and the stripline on the MMIC is equivalent to a microstrip. In this work, the distance between the bottom ground plane and the MMIC is about 250 μm, so the microstrip formula for a single ground plane was employed to calculate the Z_o of the CSP-based stripline. The open boundary closed-form equation for microstrip [11] is given by

$$Z_o = \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8h}{w_e} + \frac{w_e}{4h}\right) \left(\frac{w_e}{h} \le 1\right) \tag{1}$$

$$Z_o = \frac{120\pi}{\sqrt{\varepsilon_e}\left\{\dfrac{w_e}{h + 1.393 + 0.667\ln\left(\dfrac{w_e}{h+1.444}\right)}\right\}} \left(\frac{w_e}{h} \ge 1\right) \tag{2}$$

where ε_e, w_e, and h are the effective permittivity of the substrate, the effective width of the stripline, and the height of the MMIC substrate, respectively. Using the effective permittivity ε_e and effective width w_e of the strip line as fitting parameters, the characteristic impedance calculated from the above closed-form equation was fitted to the result of a CSP-based stripline evaluated from the EM simulation, and the values of the effective permittivity ε_e and effective width of the strip line w_e were determined by the fitting. As a result of the fitting, the permittivity ε_e was calculated as 16.3, and w_e was a simple fourth-order function of w in the range of $w = 20$–80 μm (w is the actual stripline width).

For CSP-based MIM capacitors, lumped equivalent circuits employing closed-form equations were used. A plane view and cross-sectional view of the CSP-based MIM shunt capacitor is shown in Fig. 5(a) and (b), respectively, and its lumped equivalent circuit is shown in Fig. 5(c). In the equivalent circuit, C_a corresponds to the capacitance of the shunt capacitor region [the capacitor consisting of the upper and lower electrode and the insulator, as shown in Fig. 5(b)], which is required for the shunt capacitive impedance matching. The C_a is given by

$$C_a = \frac{\varepsilon_i W H}{d_i} \text{ pF} \tag{3}$$

where ε_i, W, H, and d_i are the permittivity of the insulator, the width and height of the upper electrode, and the thickness of the insulator, respectively. C_b corresponds to the parasitic capacitance between the lower electrode and the backside metal of the MMIC, as shown in Fig. 5(b). C_b is given by

$$C_b = \frac{0.5\varepsilon_S S_L}{d_S} \text{ pF} \tag{4}$$

where ε_S, S_L, and d_S are the permittivity of the GaAs substrate, the area of the lower electrode, and the thickness of the GaAs substrate, respectively. L_a is the inductance of the parasitic inductor originating from the upper and lower electrode. The closed-form equations were determined by fitting the EM simulation result. When the width of the upper electrode W is 20 μm, L_a is expressed by the height H of the upper electrode

$$L_a = 0.543\,75(H - 52) + 6.45 \text{ pH}. \tag{5}$$

As shown in Fig. 5(c), the EM simulation data were used for the parasitic elements from the via hole and the interconnection part between the via hole and the lower electrode, which are shown in Fig. 5(a) and (b). The structure and size of the via hole and the interconnection part were fixed. Therefore, additional EM simulation is not required when the capacitance value is changed by adjusting the size of the electrodes. It is very important for the application of the model that the EM simulation parts do not change when varying the capacitance value. C_{pkg} is

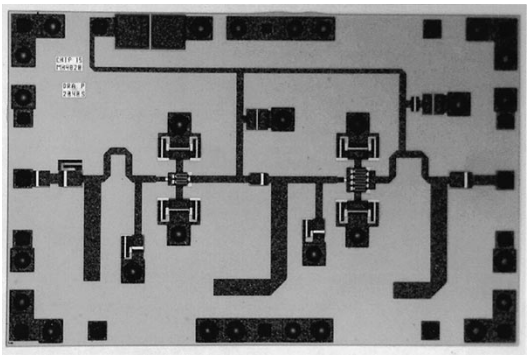

Fig. 6. Photograph of the broad-band amplifier MMIC.

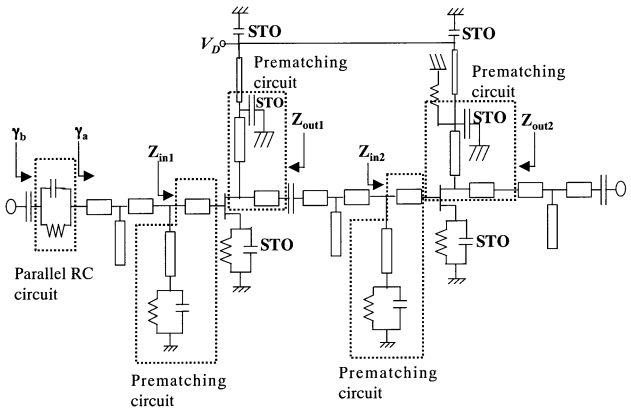

Fig. 7. Schematic circuit of the broad-band amplifier.

the parasitic capacitance originating from the ACF/Al_2O_3 layers between the upper electrode and the GND electrode of the substrate, as shown in Fig. 5(b). $C_{\rm pkg}$ is expressed as follows:

$$\frac{1}{C_{\rm pkg}} = \frac{d_a}{\varepsilon_a WH} + \frac{d_b}{\varepsilon_b WH} \ \text{pF}^{-1} \tag{6}$$

where ε_a, d_a, ε_b, and d_b are the permittivity and thickness of the ACF and the permittivity and thickness of the Al_2O_3 substrate, respectively. In this work, the distance between the GND electrode and the upper electrode is about 250 μm, and $C_{\rm pkg}$ can be ignored due to its small value. All the capacitance and inductance values of the lumped equivalent circuit are given by the above closed-form equations, which are expressed with respect to the electrode size. The scattering parameters calculated from the equations exhibited a good agreement with the results of the EM simulation. Without the EM simulation, the above equations and equivalent circuit were used for the CSP-based components during circuit design.

IV. Circuit Design

A photograph and a schematic circuit of the amplifier are shown in Figs. 6 and 7, respectively. In conventional amplifier MMICs, a lossy resistive matching technique [12], [13] and a gate-drain feedback technique [14] has usually been employed for broad-band amplifier design in the L–X-band. This matching technique resulted in a broad-band gain of the amplifier MMICs in the frequency band. In a high frequency range such as the K-band, however, the lossy resistive matching technique might cause a loss of power or a degradation of the noise characteristics, and the gate-drain feedback technique might limit the RF performance of the FET itself by reducing the maximum available gain (MAG), although they improve the stability as well as extend the bandwidth of the FET. In this work, to achieve a broad-band design (up to K-band) without the loss of high-frequency gain, a novel prematching technique employing an RC parallel circuit was used for the gate input of the FET, as shown in Fig. 7, which avoided the use of lossy matching or feedback techniques. In the relatively low frequency range of the operating band, the resistor of the parallel RC circuit contributes to band flatness and circuit stabilization by reducing the unnecessarily high gain that originates from unintended matching, such as a low-frequency resonance by bias circuits. In the relatively high frequency range of the operating band, the capacitor in the parallel RC circuit by-passes the resistor, and therefore it prevents the decrease in the high frequency gain caused by the resistor, which extends the band edge to a higher frequency. The resistance, capacitance and inductance values of the prematching circuit shown in Fig. 7 were selected using the concept of prematching. Generally, the input and output impedance of the FETs exhibit a frequency dependence due to their parasitic elements, and the frequency dependence of the reactance part of the impedance is dominant. In this work, the input and output of the FETs only shows the real part of the impedance over a wide frequency range by removing the reactance element of the FET impedance via the prematching circuits. The gate input and drain output prematching circuits from Fig. 7 connected with the parasitic elements of the FET are shown in Figs. 8 and 9. The gate input prematching circuit from Fig. 7 is connected in parallel with the parasitic elements of the gate of the FET, as shown in Fig. 8. Then L_{g1}, C_{gs}, and $R_{\rm in}$ are the parasitic inductance and capacitance of the gate of the FET and the gate input resistance of the FET, respectively, and L_{g2} is the inductance of the

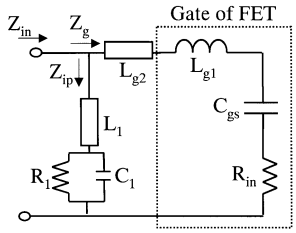

Fig. 8. Gate input prematching circuit connected with the parasitic elements of the gate of the FET.

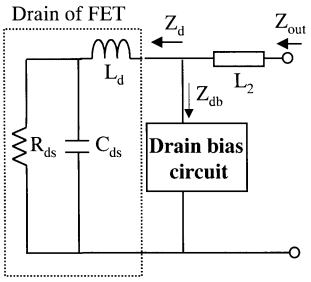

Fig. 9. Drain output prematching circuit connected with the parasitic elements of the drain of the FET.

stripline inductor, which is connected externally to increase the parasitic inductance of the FET. The gate input prematching circuit consists of the stripline inductors and the RC parallel circuit. In this case, the input impedance of the gate of the FET (Z_g), the impedance of the prematching circuit (Z_{ip}) and the total input impedance ($Z_{\rm in}$) can be expressed as follows:

$$Z_g = R_{\rm in} + j\omega(L_{g1} + L_{g2}) + \frac{1}{j\omega C_{gs}} \tag{7}$$

$$Z_{ip} = j\omega L_1 + \frac{R_1}{(1 + j\omega R_1 C_1)} \tag{8}$$

$$Z_{\rm in} = \frac{1}{\dfrac{1}{Z_g} + \dfrac{1}{Z_{ip}}} = R_{\rm in}(\omega) + j\omega X_{\rm in}(\omega) \tag{9}$$

where L_1 is the inductance of the gate stripline inductor, and R_1 and C_1 are the resistance and inductance, respectively, of the RC parallel circuit. To reduce the strong dependency of $Z_{\rm in}$ on the frequency, which originates from the parasitic elements of the gate of the FET, the reactance part $X_{\rm in}(\omega)$ should be removed. Therefore, R_1, C_1, and L_1 were selected to remove the reactance part $X_{\rm in}(\omega)$. In this case, R_1, C_1, and L_1 should satisfy the following conditions:

$$L_1 = L_{g1} + L_{g2} \tag{10}$$

$$C_1 = 2C_{gs} \tag{11}$$

$$R_1 = \sqrt{\frac{L_{g1} + L_{g2}}{3C_{gs}}}. \tag{12}$$

Since the parasitic inductor L_{g1} of the FET in Fig. 8 is too small, L_{g2} was externally connected to the FET. For the first-stage FET in Fig. 7, the values of C_1 and R_1 were 0.46 pF and 12 Ω, respectively, and the value of L_1 was 0.1 nH. For the second-stage FET in Fig. 7, the values of C_1 and R_1 were 0.9 pF and 8.5 Ω, respectively, and the value of L_1 was 0.1 nH.

The output prematching circuit is connected with the parasitic elements of the drain of the FET, as shown in Fig. 9. L_d and C_{ds}, respectively, are the parasitic inductance and capacitance of the drain of the FET, and R_{ds} is the drain resistance. The output prematching circuit consists of the drain bias circuit and the stripline inductor. The output impedance of the drain of the FET (Z_d) and the total output impedance ($Z_{\rm out}$) can be expressed as follows:

$$Z_d = \frac{R_{ds}}{1 + (R_{ds}\omega C_{ds})^2} + j\omega\left\{L_d - \frac{R_{ds}^2 C_{ds}}{1 + (R_{ds}\omega C_{ds})^2}\right\} \tag{13}$$

$$Z_{\rm out} = \frac{1}{\dfrac{1}{Z_d} + \dfrac{1}{Z_{db}}} + j\omega L_2 \tag{14}$$

where L_2 is the inductance of the stripline inductor. The drain bias circuit in Fig. 9 consists of the stripline inductors and capacitors as shown in Fig. 7. If the drain bias circuit shows a high impedance by adjusting the stripline length and the capacitance value, $1/Z_{db}$ can be ignored in (14). In this case, $Z_{\rm out}$ can be expressed as follows from (13) and (14):

$$Z_{\rm out} = \frac{R_{ds}}{1 + (R_{ds}\omega C_{ds})^2} + j\omega\left\{L_d + L_2 - \frac{R_{ds}^2 C_{ds}}{1 + (R_{ds}\omega C_{ds})^2}\right\}. \tag{15}$$

To reduce the strong dependency of $Z_{\rm out}$ on the frequency by removing the reactance part of $Z_{\rm out}$, the inductance L_2 of the strip-line inductor should satisfy the following condition:

$$L_2 = \frac{R_{ds}^2 C_{ds}}{1 + (R_{ds}\omega_c C_{ds})^2} - L_d, \tag{16}$$

where ω_c is the operating frequency. By using the above prematching circuits, the strong frequency dependence of the input and output impedances of the FETs were greatly suppressed in the operation band. The simulated input and output impedance of the first-stage FET ($Z_{\rm in1}$ and $Z_{\rm out1}$ in Fig. 7) are shown in Fig. 10(a), and the input and output impedance of the second-stage FET ($Z_{\rm in2}$ and $Z_{\rm out2}$ in Fig. 7) are shown in Fig. 10(b). As shown in Fig. 10(a), the dashed and solid lines correspond to $Z_{\rm in1}$ and $Z_{\rm out1}$, respectively. $Z_{\rm in1}$ in the frequency range from 11 to 26 GHz exists within the circumference of a circle that is located in the vicinity of 20 Ω, and $Z_{\rm out1}$ in this frequency range exists in the circumference of a circle that is located in the vicinity of 25 Ω. As shown in Fig. 10(b), the dashed and solid lines correspond to $Z_{\rm in2}$ and $Z_{\rm out2}$, respectively. $Z_{\rm in2}$ in the frequency range from 12 to 28 GHz also only reveals the real impedance values that exist in the vicinity of 10 Ω, and $Z_{\rm out2}$ in

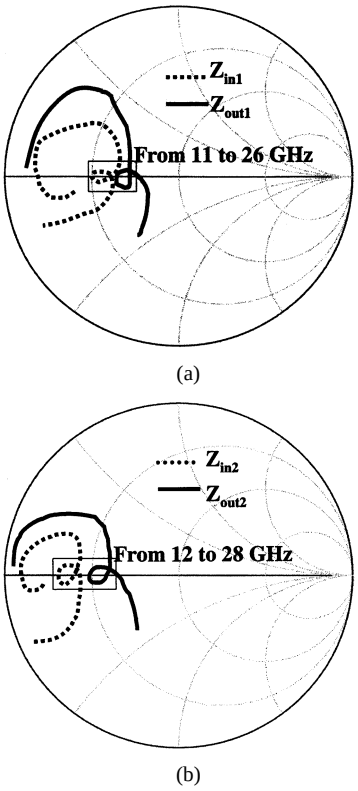

Fig. 10. (a) Simulated input and output impedance of the first-stage FET ($Z_{\rm in1}$ and $Z_{\rm out1}$ in Fig. 7). (b) Input and output impedance of the second-stage FET ($Z_{\rm in2}$ and $Z_{\rm out2}$ in Fig. 7).

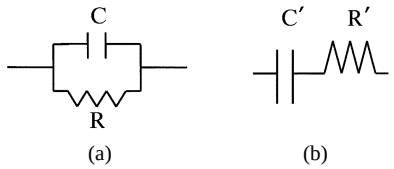

Fig. 11. (a) Parallel RC circuit. (b) Equivalent series R' C' circuit.

this frequency range reveals only the real impedance values that exist in the vicinity of 20 Ω. The impedance matching between the real impedance values of the gate input and the drain output prematching circuits was performed by open stub transformers, as shown in Fig. 7.

For the Ku-/K-band MMICs, stability should be guaranteed over a wide frequency range from dc to the operation band in order to prevent any unwanted oscillation in the out-of-band region as well as in the operation band. In this work, in order to improve the stability in the out-of-band region of the amplifier MMIC, a parallel RC circuit was connected to the input of the amplifier MMIC, as shown in Fig. 7. Without the parallel RC circuit at the input port, the K factor of the amplifier MMIC was lower than 1 in the frequency range from 10 to 11 GHz, due to the instability of the FET itself, which means that the amplifier MMIC is conditionally stable in this frequency band. Therefore, the value of resistance R for the parallel RC circuit was selected to stabilize the amplifier MMIC in the above conditionally stable frequency range by improving the input return loss in this frequency range. The value of the capacitance C was selected to bypass the resistor in the operation band or in the higher frequency range, and therefore the RF performance in the operation band is not affected by the parallel RC circuit. As shown in Fig. 11(a) and (b), the parallel RC circuit is equivalent to the series R' C' circuit, and in this case, the resistance R' and the capacitance C' can be expressed as follows:

$$R' = \frac{R}{1 + (\omega RC^2)} \tag{17}$$

$$C' = \left\{ \frac{1}{\omega^2 RC} + RC \right\} \cdot \frac{1}{R} \tag{18}$$

where R and C are the resistance and capacitance values of the parallel RC circuit, respectively. Therefore, the input return loss of the amplifier with the RC circuit (γ_b in Fig. 7) moves toward the high resistive and capacitive region by R' and C' for the parallel RC circuit. In this work, in order to improve the stability and return loss in the conditionally stable range (from 10 to 11 GHz), and to have no effect on the RF performance in the operation band (Ku- and K-band), values of 0.5 pF and 20 Ω were selected for C and R, respectively. As shown in Fig. 12, the measured return loss was plotted for the frequency range from 8 to 18 GHz, where the dashed and solid lines, respectively, correspond to the return loss of the MMIC with and without the parallel RC circuit. As shown in Fig. 12, the input return loss without the RC circuit (γ_a in Fig. 7) in the conditionally stablefrequency range moved toward the high resistive and high capacitive region (γ_b in Fig. 7) by R' and C', and therefore the input return loss was significantly improved. Fig. 13 shows the measured K factors for the amplifier MMICs, where the open circle line corresponds to the results of the amplifier MMIC with

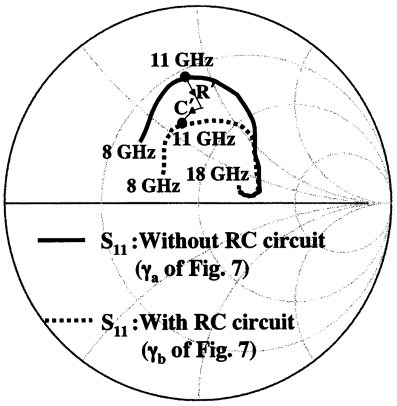

Fig. 12. Measured return loss of the amplifier MMICs in the frequency range from 8 to 18 GHz.

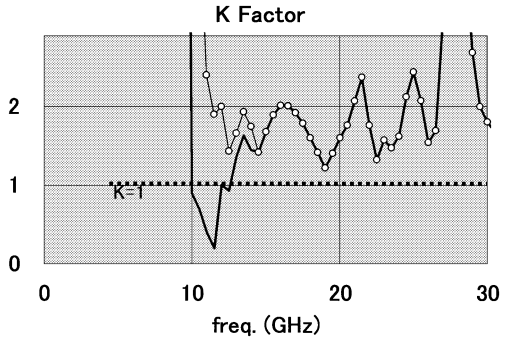

Fig. 13. Measured K factors of the amplifier MMICs.

the parallel RC circuit, and the thick solid line corresponds to the device without the parallel RC circuit. The K factors in the low frequency range were too high to plot, and these are not shown in the figure. As shown in Fig. 13, the stability over the frequency range from 10 to 11 GHz was greatly improved by the parallel RC circuit, and therefore the amplifier MMIC shows unconditional stability $(K > 1)$ in the whole frequency range.

As is well known, a high capacitance value is required for the bypass of the biasing circuit, and therefore additional biasing components are necessary on the board for the correct operation of conventional MMICs. In this work, the biasing components as well as the matching components were fully integrated on the MMIC by using a small-size STO $(SrTiO_3)$ capacitor, as shown in Fig. 7. Therefore, the packaged MMIC does not require additional matching and biasing components on the board. The STO film was deposited on a GaAs epitaxial substrate by a low-temperature RF sputtering technique, without degradation of the electrical performance of the GaAs substrate. The relative dielectric constant of the STO film is 20 times higher than that of a conventional SiN film.

A GaAs MODFET was employed as the FET in the MMIC. The length of the FET gate was 0.2 μm. The 0.2-μm gate finger was fabricated using phaseshifter-edge-line (PEL) phase-shift lithography employing a conventional i-line stepper, which is more cost-effective than an electron-beam lithography technique. The delta-doped epitaxial layer was grown on a GaAs substrate by MOCVD. The threshold voltage ($V_{\rm th}$) was −0.6 V, and the maximum transconductance $(gm_{\max})$ obtained was 625 mS/mm. The current gain cut-off frequency

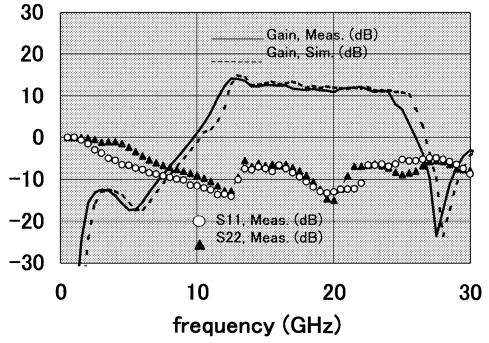

Fig. 14. Measured and simulated gain and measured return loss of the amplifier MMIC.

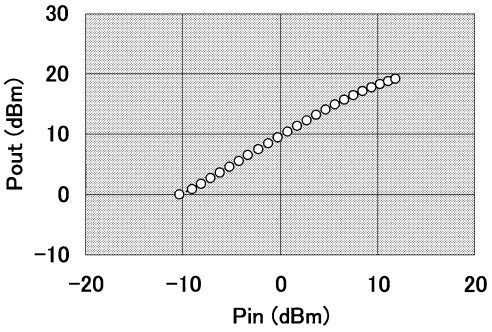

Fig. 15. Measured $P_{\rm out} - P_{\rm in}$ characteristic of the packaged MMIC at 20 GHz.

(ft) and maximum frequency of oscillation $(f_{\max})$ were 75 and 135 GHz, respectively. The gate widths (W_g) of the first- and second-stage FETs are 50×4 μm and 50×8 μm, respectively. A self-bias circuit was used to bias the FET, which requires only a single supply voltage. According to the requirement for low-power consumption in the Ku-/K-band market, the amplifier MMIC was designed for a low supply voltage of 1.5 V, although the MAG of the FETs are reduced to some extent in comparison with a high supply voltage device. For a supply voltage of 1.5 V, the measured MAG of the first- and second-stage FETs were 6.5 and 5.5 dB at 20 GHz, respectively.

V. RF Performances

The RF performance of the amplifier MMIC was measured with a supply voltage of 1.5 V. The measured and simulated gain and measured return loss of the packaged amplifier MMIC are shown in Fig. 14. The solid and dashed lines correspond to the measured and simulated gain, respectively. The open circles and solid triangles correspond to the measured input and output return loss, respectively. The measured gain exhibits good flatness over a wide frequency range. It shows a maximum value of 14 dB with 3 dB of ripple between 12 and 24 GHz, and a maximum value of 12 dB with 1 dB of ripple in the K-band (from 18 to 24 GHz), which is a value close to the summation of the MAG of the first- and second-stage FETs in the K-band. The input and output return losses show values lower than -6 dB in this frequency range. The measured $P_{1\ \rm dB}$ exhibited a maximum value of 20 dBm with 3 dB of ripple between 12 and 24 GHz. The measured $P_{\rm out} - P_{\rm in}$ characteristic of the packaged MMIC at 20 GHz is shown in Fig. 15. The measured $P_{1\ \rm dB}$ at 20 GHz is 18 dBm. The CSP solution was compared with the on-chip and surface mount package (SMP) solutions. For the on-chip solution, a two-stage bare chip amplifier MMIC without bonding wires or a package was fabricated to extract the best RF performance from the MMIC itself by removing the extrinsic loss. For the SMP solution, a two-stage amplifier MMIC was prepared with an SMP and bonding wires. Compared with the bare chip MMIC, the CSP MMIC showed a loss of 0.7 dB, which mainly originates from the interconnection region and the ACF film (as stated before, the maximum insertion loss of the CSP itself was 0.8 dB from 0 to 30 GHz). However, compared with the bare chip MMIC, the SMP MMIC with bonding wires showed a loss of 1.5 dB.

VI. Conclusion

A fully integrated broad-band amplifier MMIC employing a novel RF-CSP was developed using a novel broad-band design technology that allows for good RF performance and circuit stability over a wide frequency range. Small STO capacitors were employed for the integration of the dc biasing components on the MMIC. The packaged amplifier MMIC showed good RF performance over a wide frequency range, and good stability from dc to the operation band. Due to the cost-effective fabrication process and the compact size of the CSP MMIC, it is expected that this will be a promising candidate for application to low-cost Ku-/K-band MMICs in the wireless communication systems market.

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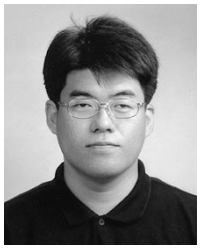

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